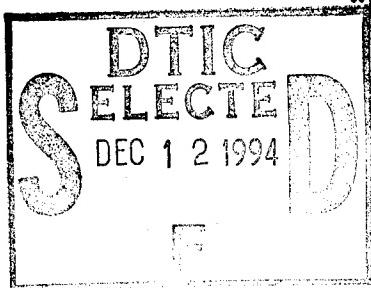


MONTHLY PROGRESS REPORT

"HTS Josephson Technology on Silicon with Application to
High Speed Digital Microelectronics"



Contract No: N00014-94-C-0261

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Summary of Progress

Task 2- RSFQ Modeling and design - We have identified parasitic inductance as a critical parameter governing the margins and performance of HTS RSFQ devices. Thermal expansion mismatch induced stress limits the overall thickness of HTS films on silicon substrates to under 70 nm. Because this thickness is less than the London penetration depth, typically 150 nm - 400 nm, we expect a substantial kinetic inductance to be associated with wiring and transmission lines. The kinetic inductance associated with the Josephson junctions themselves is still poorly understood.

Because of the importance of inductance to overall circuit performance, we have fabricated and measured (Task 3) some dc SQUIDs and RSFQ flip flops incorporating SQUIDs.

The estimated sheet parasitic kinetic inductance is given by the formula $L_{sq} = \lambda_L^2/d$, where λ_L is the London penetration depth, d is the film thickness ($d \ll \lambda_L$) and the current distribution is assumed to be uniform. The total loop inductance in a dc squid can be extracted from the magnitude of the magnetic field induced critical current modulation. We have performed measurements on a SQUID fabricated from a 25 nm thick film grown on an LaAlO_3 substrate by the barium fluoride process. The inductance calculated over a wide temperature range are plotted in Figure 1. Similar results for a much smaller SQUID imbedded in an RSFQ flip flop are also shown in the figure.

The temperature dependence to the sheet inductance is a signature of substantial kinetic inductance. Since kinetic inductance negatively impacts circuit performance, it is essential that careful quantitative account of all sources of inductance be included in circuit design efforts.

The results indicate that kinetic inductance will be a significant hurdle to the success of HTS RSFQ devices, but that, at least for now, the inductance is low enough to proceed, and we are developing plans to improve our film technology to reduce the impact of parasitic inductance.

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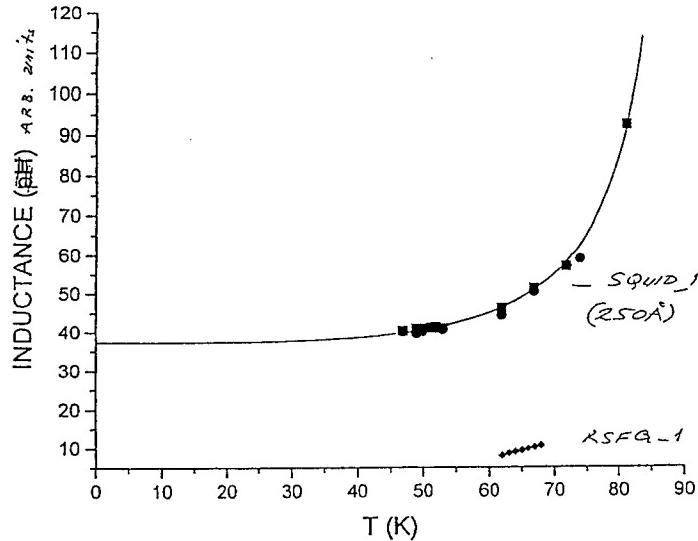


Figure 1. Temperature dependent SQUID inductance for two devices.

Task 3 - RSFQ circuit fabrication and testing - We have fabricated dc SQUIDs and an RSFQ flip flop incorporating several SQUIDs using the AT&T Barium flouride process on LaAlO_3 substrates. The films were 25 nm thick. The magnetic field dependence of the critical currents and the modulation depth as a function of bias and temperature were measured. Analysis of these measurements is currently underway. Figure 2 shows the current modulation depth as a function of bias voltage for a SQUID imbedded in an RSFQ flip flop at 66 K. The measurements show nearly a 50% modulation in current at low bias voltages, an encouraging result.

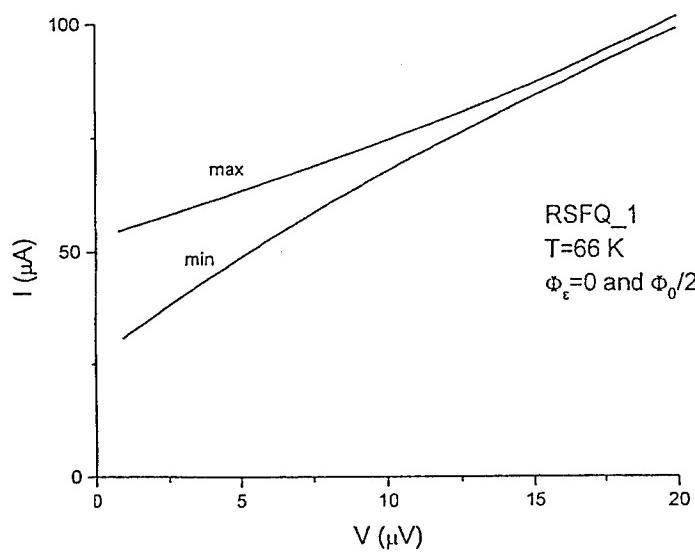


Fig. 2 Measured modulation depth of a thin film HTS SQUID in an RSFQ logic element.

We are investigating a new approach to improved buffer layers that will allow relaxation of thermal expansion mismatch induced stress in HTS thin films on silicon. If successful, the new buffer layers will enable the growth of significantly thicker films and multilayered structures. The new buffer layers fabricated using glass films with low annealing points incorporated in a wafer bonding scheme.

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